GAIN CONTROLLABLE VERY LOW VOLTAGE (≤ 1 V) 8-9 GHz INTEGRATED CMOS LNA'S

Tommy K. K. Tsang and Mourad N. El-Gamal
Microelectronics And Computer Systems Laboratory, McGill University
3480 University Street, Montreal, Quebec, Canada H3A 2A7
E-mail: {ktsang, mourad}@macs.ece.mcgill.ca

Abstract - **This paper presents the design and experimental results of two CMOS low-voltage low noise amplifiers intended for future wireless applications, and featuring a new and very simple gain control mechanism. Implemented in a standard 0.18 μm CMOS process, and operating from a supply voltage of 1 V, the 8 GHz LNA exhibits a power gain of 13.7 dB and a noise figure of 3.2 dB, while the 9 GHz LNA achieves a forward transmission S_{21} of 12.2 dB and a noise figure of 3.7 dB. Both circuits have a gain tuning range of over 10 dB, and can operate from a supply voltage as low as 0.7 V.**

I. INTRODUCTION

CMOS technology would be the technology of choice for wireless applications, provided it is able to meet the overall system specifications, mainly attributed to its lower cost, lower power, and higher level of integration with baseband digital circuitry. As the minimum feature size of CMOS devices decreases, the RF performance (e.g. f_T) continues to improve and gets closer to those of GaAs and SiGe, in the low GHz range. Deep sub-micron CMOS devices with f_T's exceeding 100 GHz and minimum noise figures less than 0.5 dB at 2 GHz have been realized [1].

Driven by the insatiable demand for larger bandwidth, wireless standards are constantly evolving towards higher carrier frequencies, thus driving the research focus of CMOS RFIC's higher into the GHz range (e.g. [2]-[6]). Wireless applications were developed for the 900 MHz and 1.8 GHz bands, followed by the current 2.4 GHz Bluetooth applications, then the 5-6 GHz bands for wireless LAN systems (e.g. IEEE 802.11a and HIPERLAN). Future technological advances and demands anticipate the use of CMOS technology, operating at higher frequency bands (e.g. 5-10 GHz), for next generation wireless communications applications.

This paper is the first to demonstrate CMOS LNA's for the 8-9 GHz range, operating with a voltage supply of 1 V, and with over 10 dB of gain control. Two prototypes were implemented in a standard 0.18 μm CMOS process. The main difference between the two prototypes is the use of different inductor structures. Both LNA's are intended for integration within a complete system-on-chip (SoC) transceiver.

The following section introduces the low-voltage topology chosen, and provides details of design equations and constraints. Section 3 addresses inductor design guidelines and layout techniques to yield an optimal performance in CMOS at GHz frequencies. Finally, the paper concludes with experimental results and a performance summary of the two prototypes under different biasing conditions.

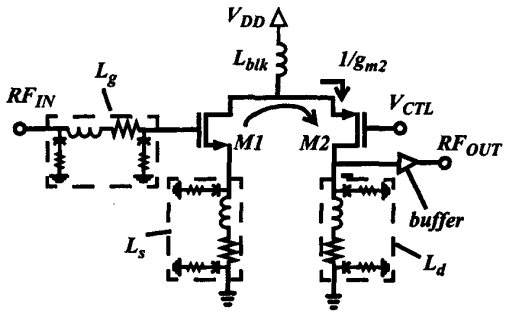

Fig. 1: Schematic of the gain controllable sub-1 V LNA.

II. LNA TOPOLOGY AND DESIGN EQUATIONS

With the targeted voltage supply down to 1 V, there are limited numbers of suitable LNA topologies. Conventional cascode amplifiers require a relatively high supply voltage headroom, while single transistor amplifiers are prone to instability problems. A low-voltage (1 V) bipolar design using capacitively coupled LC tanks has been demonstrated in [7], but matching two coupled LC tanks to resonate at the same frequency of interest, with other stringent design requirements met, is challenging. The proposed low-voltage design is based on a folded cascode topology (Fig. 1). A simple gain tunability mechanism for this structure is suggested for the first time. Since the LNA is used for narrowband applications, an LC resonant tank is used (i.e. L_{blk} and parasitic capacitances), exhibiting a high impedance at RF and forcing the signal current ($g_{m1}v_{gs1}$) into the source of transistor M2 (driving $1/g_{m2}$).

A. INPUT IMPEDANCE AND NOISE MATCHING

Input matching is an important design issue, necessary to minimize signal reflection and noise. There is often a trade-off between noise and input impedance matching in LNA designs. This trade-off reflects on the choice of transistor sizing, which is mainly dependent on the designer's objectives and priorities. A common approach used is to first determine the transistor sizing which makes the circuit be approximately noise matched to the characteristic impedance of the system, typically 50 Ω, at the frequency of interest. Then, a minimal passive network is added to fine tune the input matching. In this design, a common series-connected two-element matching network is used, as shown in Fig. 2: It consists of gate and source inductors L_g and L_S, respectively.

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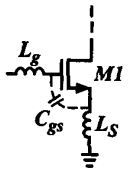
The source degeneration inductor L_S is used to match the real part of the input impedance to the characteristic impedance of the system ($Z_s = 50\,\Omega$), while the combination of source and gate inductors are used to cancel out the reactance due to the parasitic capacitance C_{gs} of the input transistor M1. The conditions for input impedance matching (Z_{in}), and the expression for the resonant frequency ω_o are summarized as follows:



$$Z_{in} = s(L_S + L_g) + \frac{1}{sC_{gs}} + \left(\frac{g_{m1}}{C_{gs}}\right)L_S \approx \left(\frac{g_{m1}}{C_{gs}}\right)L_S = \omega_T L_S \text{ (at resonance)}, \quad (1)$$

$$\omega_o = \frac{1}{\sqrt{(L_g + L_S)C_{gs}}}. \quad (2)$$

Fig. 2: Input impedance matching network.

Since a prime objective of this work is noise minimization, the matching network is designed to achieve the minimum overall noise figure, while still maintaining a reasonable input impedance matching, at the frequency of interest.

B. Gain Controllability

Linearity is becoming an important system design issue in today's wireless applications. Narrower allocated channel spacing drives the need for high linearity (i.e. IIP3), in addition to good noise and gain performance. Since high linearity trades off with high gain, the controllability of the latter becomes a very desirable feature in modern LNA designs. This can enhance the IIP3 by decreasing the gain at high input-power levels. It also relaxes both the linearity requirements of other blocks in the receiver chain, and the dynamic ranges of the on-chip variable gain amplifiers (VGA's) at latter stages.

There exists several types of variable gain LNA solutions in the literature (e.g. [8]-[9]): They include i) a switch-control type, which provides gain control by switching on/off active gain components, ii) and the two-stage LNA-VGA type, which achieves gain control through the use of a VGA as a second stage. This additive gain-control functionality comes at a price of higher circuit complexity, which also results in an increase in power consumption and noise degradation.

One of the advantages of the solution proposed in this paper, over existing VGA designs, is its simplicity. The only increase in the LNA circuit complexity is an extra gain-control signal, V_{CTL}, as shown in Fig. 1. Gain variation is achieved by controlling the gate voltage of the PMOS transistor M2, hence adjusting the overall gain of the LNA *without affecting the optimum input noise and impedance matching,* which are set by the input NMOS transistor M1. A reasonably low noise figure can be achieved while providing gain controllability. Conventional cascode amplifiers do not have this flexibility in gain-control, since the overall gain of the LNA is governed by the input transistor M1, while the cascode transistor M2 only acts as a current buffer. Gain control could only be achieved by altering the biasing current through M1, and consequently affecting the whole input noise and impedance matching, which is definitely not desirable.

III. Circuit Optimization

Designing RF circuits operating at frequencies greater than 1 GHz in a standard CMOS process imposes many challenges and difficulties. Iterative circuit optimization is often necessary. In this section, a summary of inductor design guidelines and layout techniques, which have been adopted in this work, is presented.

A. Integrated Inductor Design Guidelines in CMOS

Proper modeling of integrated inductors at radio frequencies is one of the most challenging and crucial tasks in LNA design. Standard CMOS integrated inductors have inherently low quality factors (i.e. $Q < 5$) since they exhibit serious substrate and dielectric losses, which become dominant at GHz frequencies. This is mainly due to the high conductivity of the CMOS substrate. Substantial research efforts have been invested into this topic recently, attempting to improve the accuracy of inductor modeling and the quality factors of inductors in a CMOS technology. The main objective of this section is to provide practical guidelines, and point out the trade-offs in inductor design in CMOS for RF.

Based on earlier work from the literature on inductor design (e.g. [10]-[11]), there are a number of ways to implement integrated inductors. Apart from the key geometrical parameters such as conductor width (W), number of turns (N), and inductor shape, the use of patterned ground shields and multi-layer structures are other inductor design issues. Since the targeted operating frequencies in this work are above 8 GHz, the prime objective is to design inductors with a high quality factor (i.e. $Q > 5$) at those frequencies, and to simultaneously maximize their self-resonance frequencies, f_{RES}, by pushing them much higher than this range.

Although the use of a patterned ground shield would reduce Eddie current losses at high frequency, and improve the quality factor, it can significantly reduce the f_{RES} of an inductor due to the additional capacitive parasitics it introduces. Hence, in this work, a patterned ground shield is not inserted between the spiral inductor and the silicon substrate. Furthermore, a multi-layer structure is not necessary since the required inductance for this frequency range (8-9 GHz) is only in the order of 1 to 1.5 nH, which can be easily implemented with a simple planar structure. In order to achieve high Q through reducing the series resistance, the number of turns (N) should be minimized, while the conductor width (W) should be made large. However, increasing W can have a negative effect on the self-resonance frequency, since wider metal traces translate

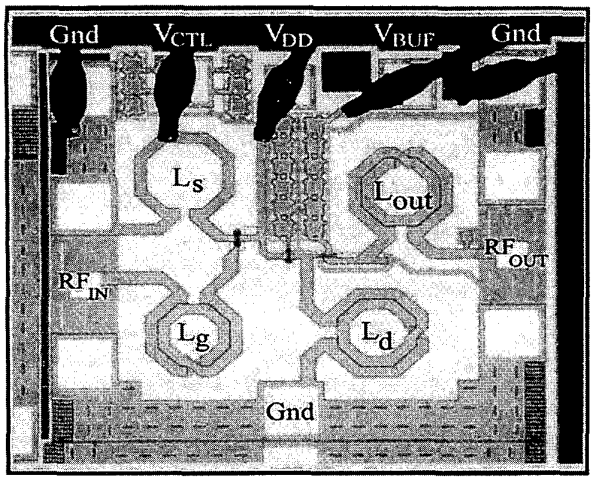


Fig. 3: Microphotograph of the 9 GHz CMOS LNA.

into a larger parasitic capacitance to substrate. There exists an optimum value for W, which we found to be 20 μm. This conclusion was reached and verified by both simulation and experimental data [12]. Finally, to further reduce the series resistance of the inductor, more than one metal layer are used to emulate a thicker conductor. Namely, the top two metal layers are used for the 8 GHz LNA, while the top three layers are used for the 9 GHz LNA. All the inductors used in both prototypes are expected to have quality factors greater than 5 in the 8-9 GHz frequency range, and are octagonal in shape.

B. RF Layout Techniques

Layout is another important step in optimizing a high frequency design. Poor layout could result in large discrepancies between the actual and expected performance, or even result into a non-working circuit. The microphotograph of the 9 GHz CMOS LNA is shown in Fig. 3. The total chip area, including the bonding pads, is 1 mm by 0.9 mm.

Careful layout is observed in order to maximize performance. The layout is done in a uni-directional fashion, i.e. no signal returns close to its origin, to avoid coupling back to the input. The RF input and output ports are placed on opposite sides of the chip to improve port-to-port isolation. Since on-chip probing is used to measure the LNA's performance, standard Ground-Signal-Ground (GSG) configurations are used at both the input and output RF ports. In order to minimize the effect of substrate noise on the system, a solid ground plane, constructed using a low resistivity metal-1 material, is placed between the signal pads (metal-6) and the substrate.

Since the operation of inductors involves magnetic fields, they can affect nearby signals and circuits, and cause interference. Therefore, inductors are placed far apart from each other, as well as from the main circuit components, with reasonable distances. Many ground connections to substrate are located near all inductors to reduce substrate noise. Furthermore, traces connected to all inductors are made wide enough to minimize series parasitic resistances and inductances, and thus avoid inductor Q degradation. Finally, line widths are set according to RF design guidelines, keeping DC traces thin and AC connections wide and as short as possible.

IV. Measured LNA's Performances

The scattering parameters of the LNA prototypes were measured on wafer using GGB Industries Inc. picoprobes and a 20 GHz Agilent 8720ES vector network analyzer. The forward transmission (S_{21}) plots of the 8 GHz and 9 GHz circuits are shown in Fig. 4 and Fig. 5 respectively. With a power consumption of around 20 mW from a 1 V supply, both prototypes achieved a power gain of 12-13.5 dB at the frequency of interest, with a noise figure of 3.2-3.7 dB. The input and output reflection coefficients of the two prototypes are below -5 dB and -13 dB respectively. Both LNA's exhibit a power gain greater than 5 dB at an extremely low voltage supply of 0.7 V, with a power consumption of around 10 mW. The performance summary of the two LNA's under different conditions are shown in Table 1, and compared to the LNA in [5]. The gain tuning characteristics are shown in Fig. 6. A gain control of over 10 dB is achieved without any increase in circuit complexity (section 2).

Despite of the higher operating frequency of the 9 GHz LNA, it has a relatively narrower bandwidth when compared to the 8 GHz LNA. This is mainly due to the use of combined three metal layers (metal 4-6) for the inductors in the 9 GHz prototype as opposed to the top two metal layers (metal 5-6) used in the 8 GHz LNA. This supports the fact that inductors with higher Q can be realized in CMOS by stacking more metal layers to emulate thicker conductors.

V. Conclusion

We have presented a topology, which has been demonstrated by experimental results, to be suitable for low-voltage ($\leq$ 1 V), high frequency ($>$ 7 GHz) LNA's, featuring a new and very simple gain controllability mechanism. Two prototypes were implemented in a standard 0.18 μm CMOS process, operating at the frequencies of 8 GHz and 9 GHz. Both LNA's achieved a power gain greater than 12 dB from a 1 V supply, with over 10 dB of gain tuning range, and 3-4 dB of noise figure. Inductor design guidelines and trade-offs, as well as RF layout techniques for performance optimization, have been addressed. Both LNA's are intended for complete integration within a low voltage transceiver for next generation wireless applications.

VI. Acknowledgment

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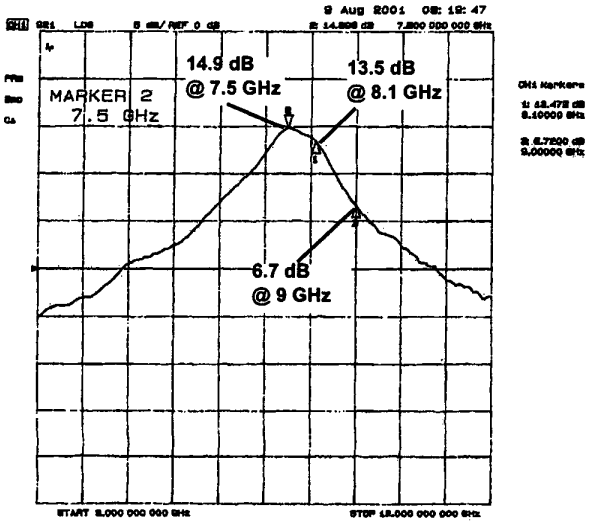

Fig. 4: The power gain of the 1-V, 8 GHz CMOS LNA.

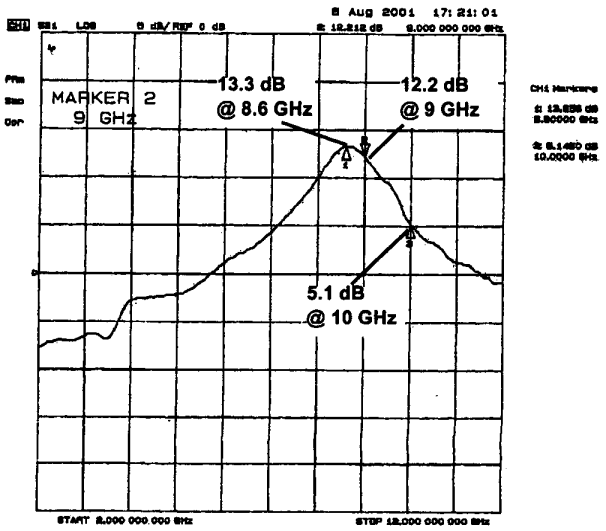

Fig. 5: The power gain of the 1-V, 9 GHz CMOS LNA.

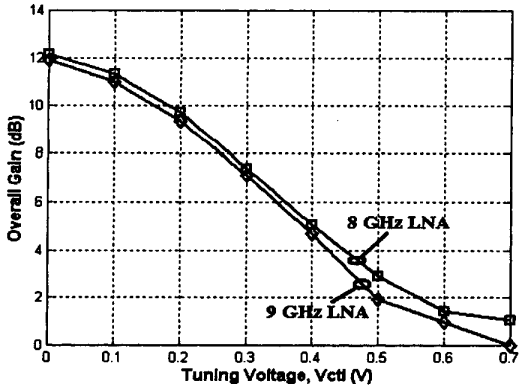

Fig. 6: Gain tuning characteristics of the LNA's, with 1-V supply.

	Prototype 1 8GHz LNA		Prototype 2 9GHz LNA		[5] 7GHz LNA
Technology	CMOS 0.18um	CMOS 0.18um	CMOS 0.18um	CMOS 0.18um	CMOS 0.25um
V_{dd}	1 V	0.7 V	1 V	0.7 V	2 V
S_{21}	13.5 dB	7.1 dB	12.2 dB	5.2 dB	6.2 dB
S_{11} / S_{22}	-5.8 / -13.9 dB	-10.9 / -17 dB	-5.4 / -11.9 dB	-9 / -12.9 dB	-
P_{dd}	22.4 mW	10.7 mW	19.8 mW	9 mW	13.8 mW
$NF_{50\ ohm}$	3.2 dB	4.1 dB	3.7 dB	4.7 dB	3.3 dB
P_{1dB}	-13.2 dBm	-8.6 dBm	-8.7 dBm	-4.3 dBm	-1.6 dBm
Gain Tuning	11.4 dB's	7.1 dB's	11.2 dB's	5.2 dB's	-

Table 1: Performance summary of the two CMOS LNA prototypes, and comparison to [5].